

LINEAR POWER AMPLIFIER WITH MULTIPLE OUTPUT POWER LEVELS

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ABSTRACT

A power amplifier stage has a first amplifier subsection and a second amplifier subsection coupled in a parallel configuration. The first amplifier subsection receives a signal to be amplified and the second amplifier subsection receives the signal to be amplified via a first delay line. The amplified output signal of the first amplifier subsection is passed through a second impedance inverter and is combined with the amplified output signal from the second amplifier subsection. In a low power mode, the first amplifier subsection operates as a linear amplifier and the second subsection is biased off. In a high power mode, both the first and second amplifier subsections operate as linear amplifiers. Selecting the impedances of the second delay element and the first amplifier to be equal is essential for high power mode operation and greatly improves the amplifier efficiency in the low power mode.